OIPE IAP19
JUN 20 2006
PATENT & TRADEMARK OFFICE

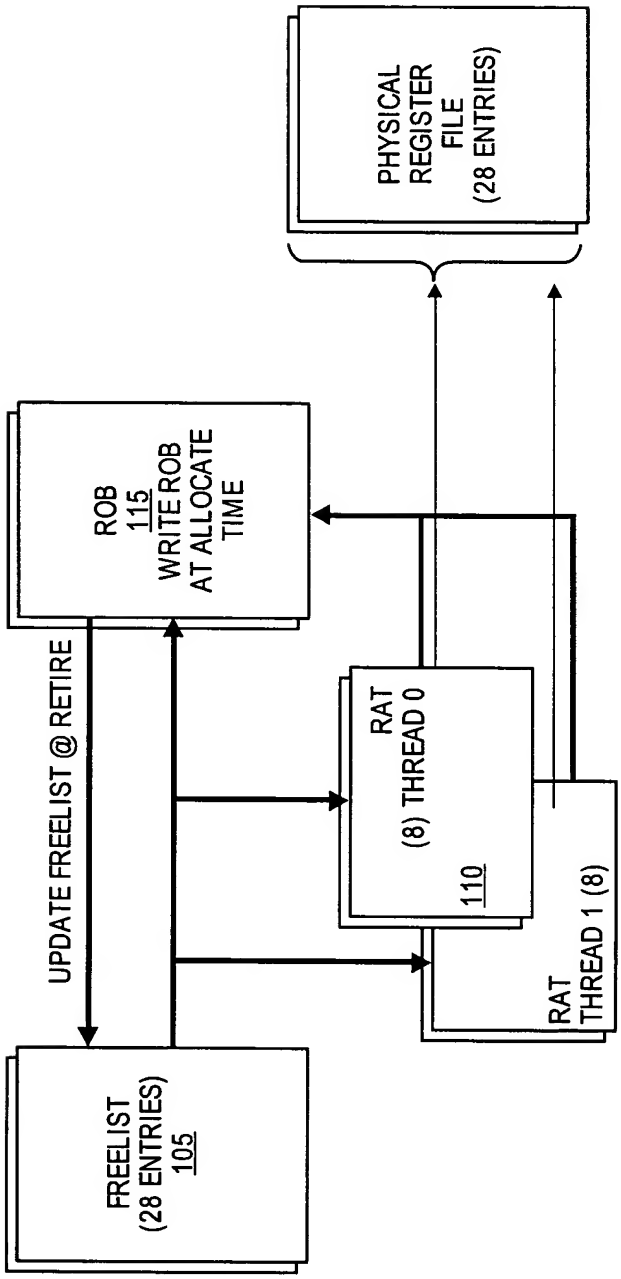

FIG. 1
(PRIOR ART)

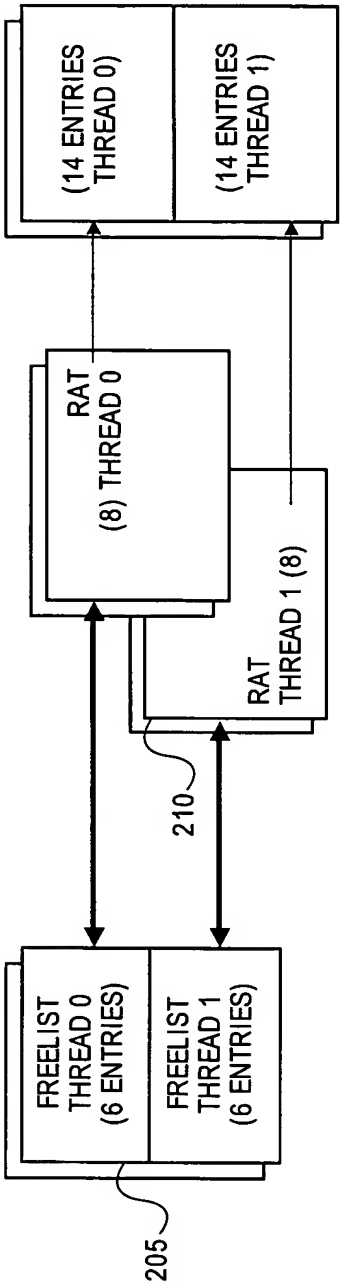

FIG. 2
(PRIOR ART)

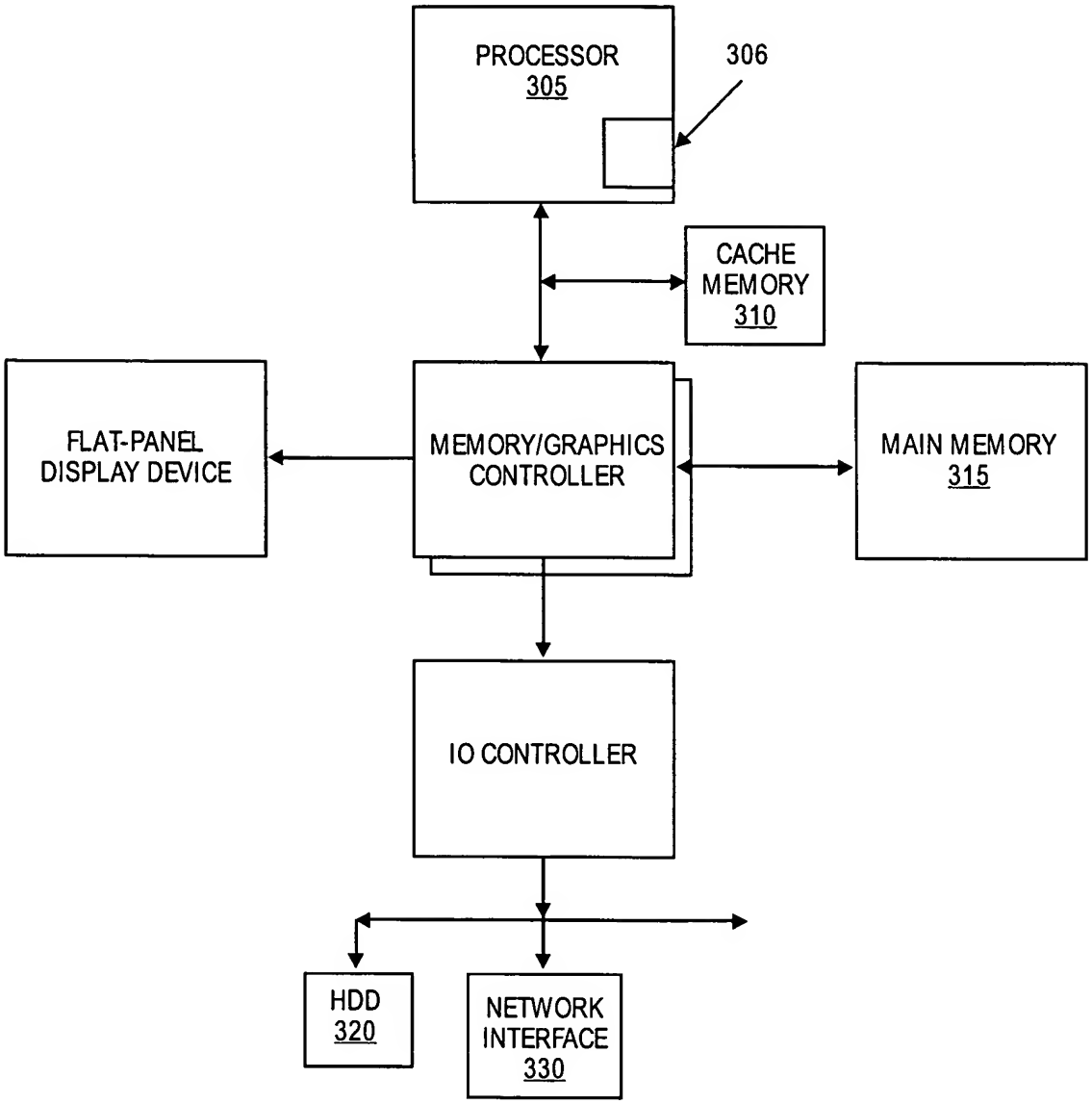
PROCESSOR
305
306
CACHE
MEMORY
310
FLAT-PANEL
DISPLAY DEVICE
MEMORY/GRAPHICS
CONTROLLER
MAIN MEMORY
315
IO CONTROLLER
HDD
320
NETWORK
INTERFACE
330

FIG. 3

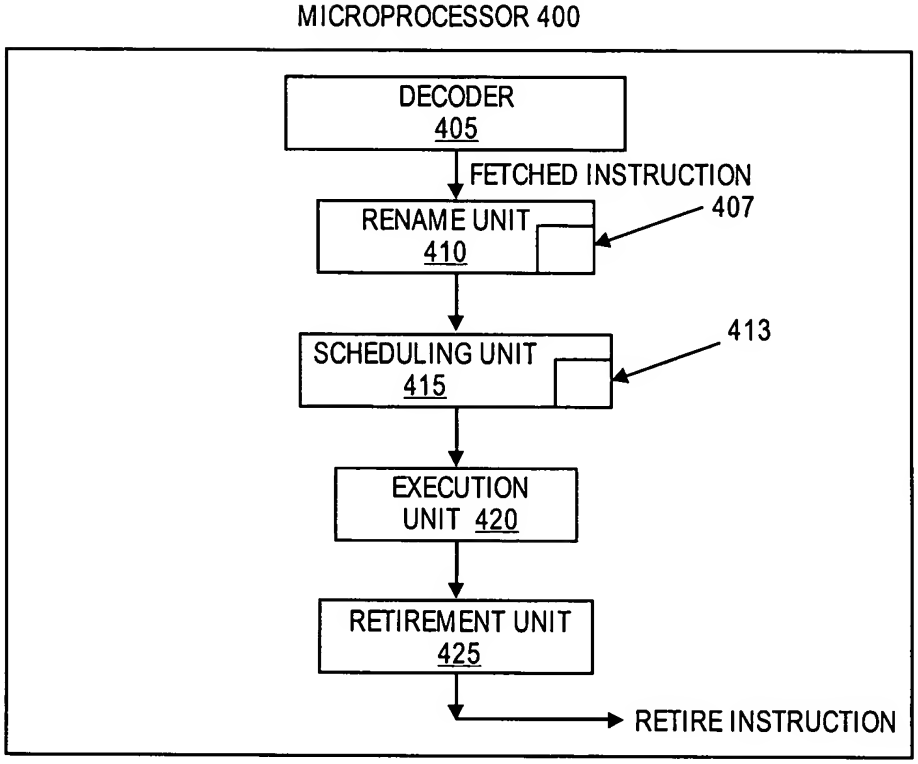
MICROPROCESSOR 400
DECODER
405
FETCHED INSTRUCTION
RENAME UNIT
410
407
SCHEDULING UNIT
415
413
EXECUTION
UNIT 420
RETIREMENT UNIT
425
RETIRE INSTRUCTION

FIG. 4

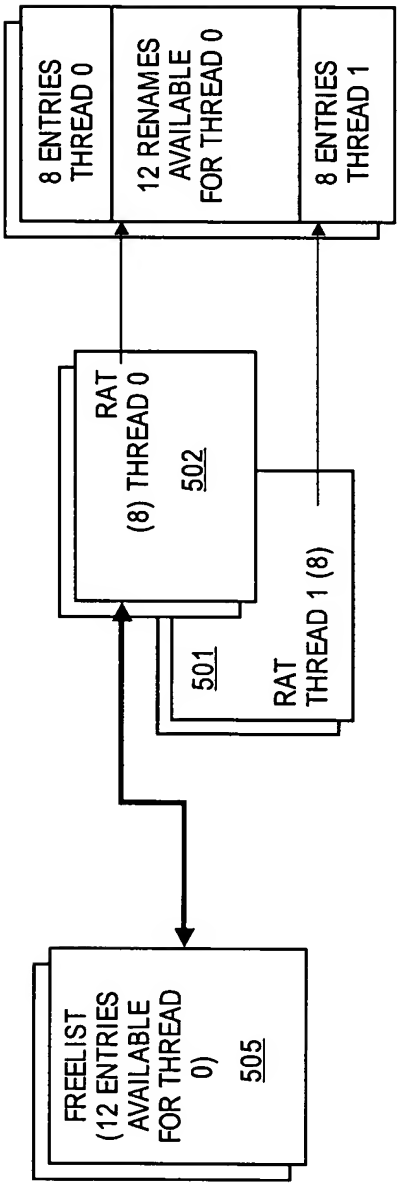
8 ENTRIES THREAD 0
12 RENAMES AVAILABLE FOR THREAD 0
8 ENTRIES THREAD 1
RAT (8) THREAD 0
502
501
RAT THREAD 1 (8)
FREELIST (12 ENTRIES AVAILABLE FOR THREAD 0)
505

FIG. 5

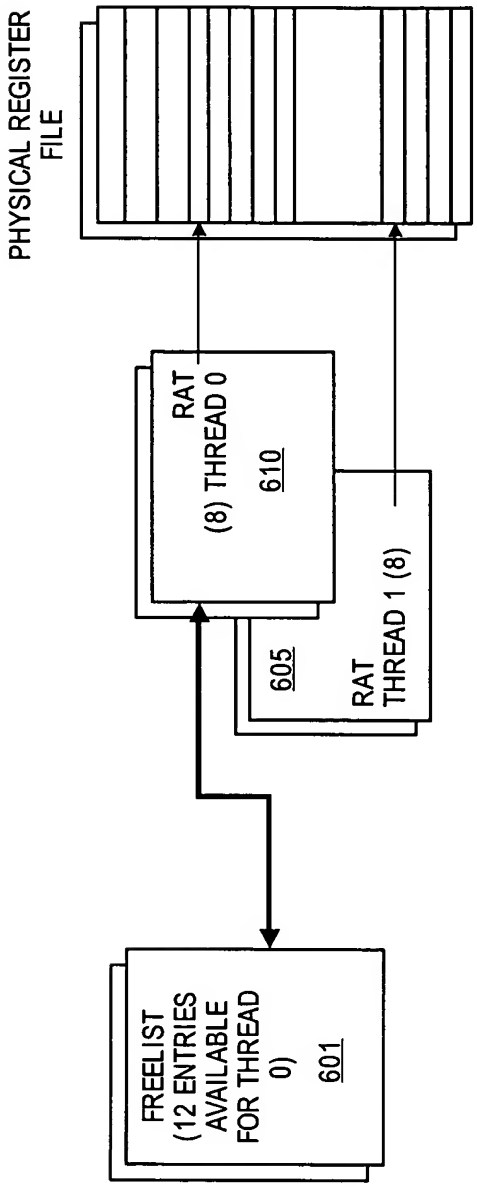
PHYSICAL REGISTER FILE
RAT (8) THREAD 0 610
605
RAT THREAD 1 (8)
FREELIST (12 ENTRIES AVAILABLE FOR THREAD 0) 601

FIG. 6

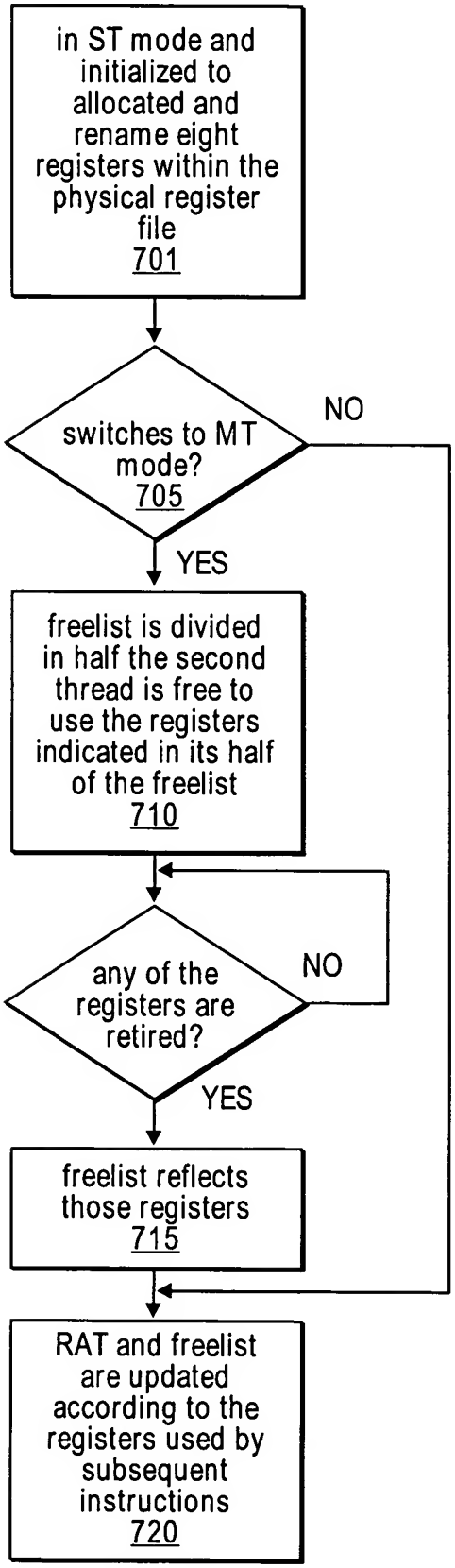
in ST mode and initialized to allocated and rename eight registers within the physical register file
701
switches to MT mode?
705
NO
YES
freelist is divided in half the second thread is free to use the registers indicated in its half of the freelist
710
any of the registers are retired?
NO
YES
freelist reflects those registers
715
RAT and freelist are updated according to the registers used by subsequent instructions
720

FIG. 7